2.6 A 40mW 3.5kΩ 3Gb/s CMOS Differential Transimpedance Amplifier Using Negative-Impedance Compensation

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The parasitic capacitance appearing at the input of a TIA has been shown to have significant impact on the receive performance. The input capacitance is due to the integrated photodiode (PD), the TIA, the bondpad, and the ESD protection circuit. To achieve a larger input capacitance tolerance, conventional approaches such as the multi-stage topology [1] and the regulated cascode topology [2], focus on reducing the effective input impedance of the TIA. However, this results in increased power consumption and poor noise performance. Recently, the self-compensated differential TIA topology that uses the bootstrapping technique combined with a differential-sensing scheme has been shown to be very effective at cancelling the loading effects caused by both the PD and the ESD protection circuit [3]. However, to make this design topology feasible for advanced CMOS technology, additional bandwidth-enhancement techniques must be used to overcome the limitations caused by the low supply voltage. Compared to the peaking techniques using inductors, the negative-impedance compensation (NIC) technique using active circuits has been shown to be more flexible and cost-effective [4]. In this paper, an inductor-free design approach that incorporates both the self-compensated topology and the NIC technique is realized in a 0.18μm CMOS technology at a 1.8V supply.

Figure 2.6.1 shows the complete circuit diagram of the proposed self-compensated differential TIA IC. The transistor M_1 plays the most important role in providing the desired capacitance cancellation. It not only serves as a voltage follower capable of reducing the transient signal across the PD, but also acts as a unity-gain current buffer to pass the photocurrent to the non-inverting input of the following core differential TIA, T_1. The differential-sensing scheme improves the transimpedance gain by a factor of 2 and also potentially increases the sensitivity.

To achieve automatic offset cancellation (AOC), dual-loop feedback circuits comprising 2 comparators and 2 controllable current sources, are included. The AOC not only reduces waveform distortion, but also improves the overload characteristic. The resulting lower cut-off frequency is around 50kHz in the proposed design. A simple RC network, comprising R_C and C_C, is used to provide both the AC-coupling path required for the capacitance cancellation and the DC control of the reverse bias voltage for the PD, to guarantee an optimized operating bandwidth. A voltage headroom of about 1.2V is reserved for the PD. As a result, voltage headroom for the core differential TIA, T_1, is reduced to about 0.3V. To overcome the headroom limitation, the 2 comparators used for achieving AOC are designed with built-in offset voltage, V_{OS}, of about 0.3V. Hence, the voltage headroom for the output of the core differential amplifier is doubled and the design constraints are relaxed.

Following the core circuit, a wideband gain stage and an output buffer capable of driving 50Ω loads are included. The capacitors C_1 and C_2 are used to serve as the loading capacitances caused by the ESD-protection circuits. By controlling the switches connecting to the capacitors, their impact on the receive performance can be investigated directly.

Figure 2.6.2 shows the circuit diagram of the core differential TIA, T_1, incorporating the NIC. A differential pair with constant feedback resistors is used to serve as the main amplifier due to its excellent noise characteristic and phase margin. However, the low open-loop gain makes it difficult to achieve a high gain-bandwidth product. In general, active loads can be employed instead of resistors to boost the amplifier gain. However, it inevitably results in degraded dynamic range due to the poor linearity of the active load. To enhance the gain-bandwidth product, both negative resistance and negative capacitance are used to adjust the output impedance of the main amplifier. Compared to the single-ended design in [4], the implementation of differential NIC is much easier. Moreover, due to the extra voltage headroom achieved by the 0.3V built-in offset voltage, V_{OS}, larger loading resistance can be used for the main amplifier. The resulting higher output impedance also makes the implementation of the NIC easier. In addition, the larger voltage headroom also results in a larger dynamic range. To control the common-mode voltage of the output, additional feedback circuits consisting of a resistor string, a comparator and a controllable current source are included.

To achieve wideband performance, the active feedback technique [5] combined with negative-capacitance compensation is used for the design of the gain stage and a f_t-doubler is used for the output buffer. Figure 2.6.3 shows their circuit diagrams.

For optical tests, the differential TIA IC is integrated with a commercial InGaAs PIN PD in a chip-on-board assembly. The active area of the PD is 70μm in diameter. The PD capacitance is around 0.8pF under 1.2V reverse-bias voltage and its corresponding responsivity is 0.9A/W at a wavelength of 1310nm. With a 2^{31}-1 PRBS, the extinction ratio of the 1310nm optical transmitter is about 10dB. With both C_1 and C_2 enabled, Fig. 2.6.4 shows the measured optical eye diagram under input optical power of -15dBm at 3Gb/s. Figure 2.6.5 shows the measured BER versus input optical power at 3Gb/s. For the BER measurement, the output signal of the optical receiver is amplified by a wideband post-amplifier with voltage gain of 40dB before it is sent into the BER tester. At a BER of 10^{-12}, the sensitivity is slightly degraded from -20.3 to -20dBm due to the combined loading effect of both C_1 and C_2. Figure 2.6.6 shows the measured eye diagram under input optical power of +0dBm at 3Gb/s. The dynamic range of the optical receiver is greater than -20dBm to 0dBm without using gain control. By disabling the NIC circuit, the enhancement achieved by the NIC can be investigated experimentally. The results show a gain enhancement factor of 70% accompanied by an enhancement factor of greater than 2 on the operating speed. Experimental tests show that the combined loading effect of C_1 and C_2 on the eye diagram is almost negligible.

The measured differential transimpedance gain is 3.5kΩ without any stability problem. The measured maximum differential output swing is 570mV$_{pp}$. The complete TIA IC consumes 40mW from a 1.8V supply. The TIA core uses 8mW and the rest of the chip uses 32mW. Figure 2.6.7 shows the die micrograph of the TIA IC. It occupies 560×400μm^2 and the active area excluding the decoupling capacitors is about 100×100μm^2.

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References:
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[5] S. Galal and B. Razavi, "10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138-2146, Dec., 2003.

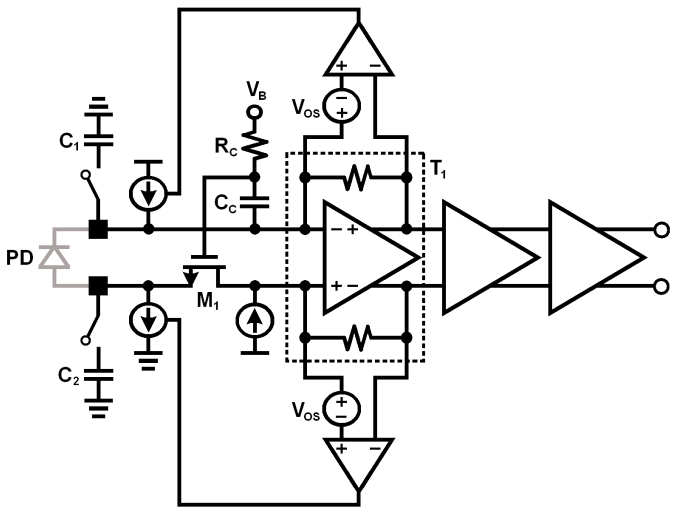

Figure 2.6.1: The self-compensated differential TIA IC.

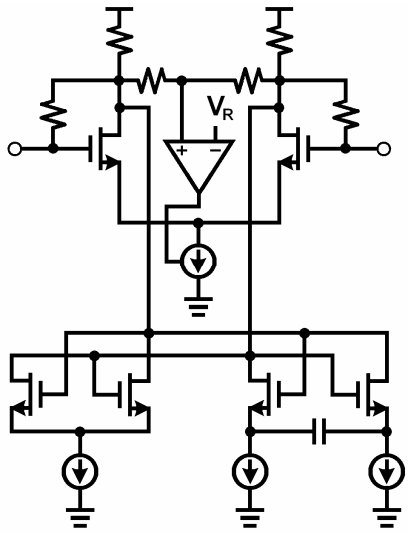

Figure 2.6.2: The core differential TIA.

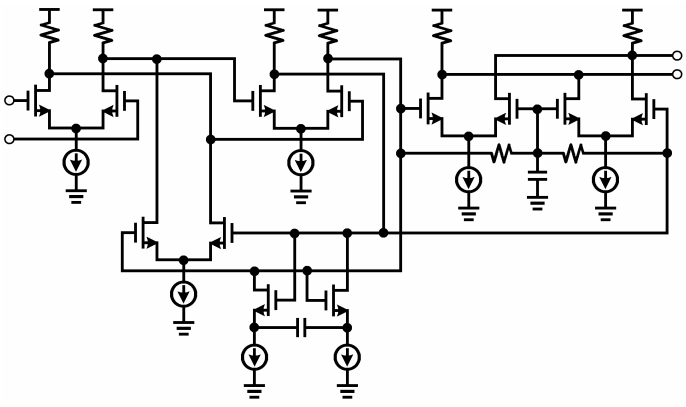

Figure 2.6.3: The gain stage and the output buffer.

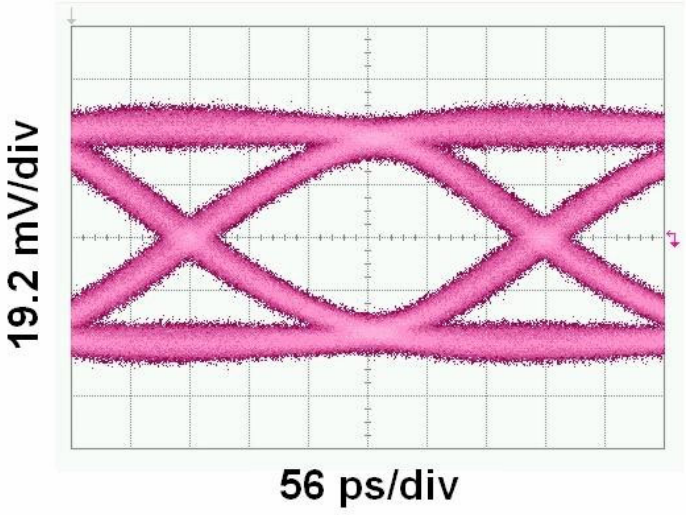

Figure 2.6.4: Measured eye diagram under input optical power of -15dBm at 3Gb/s.

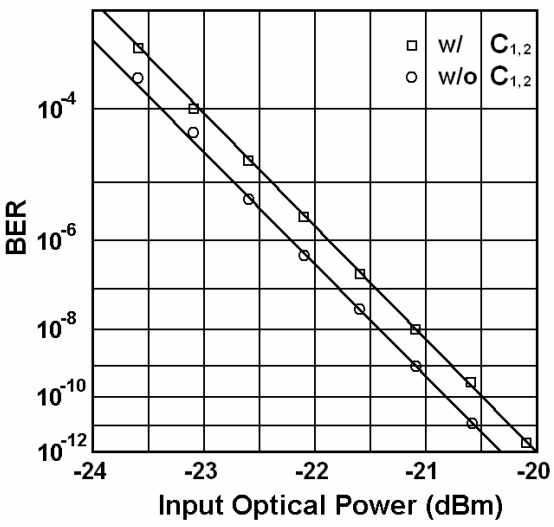

Figure 2.6.5: Measured BER versus input optical power at 3Gb/s.

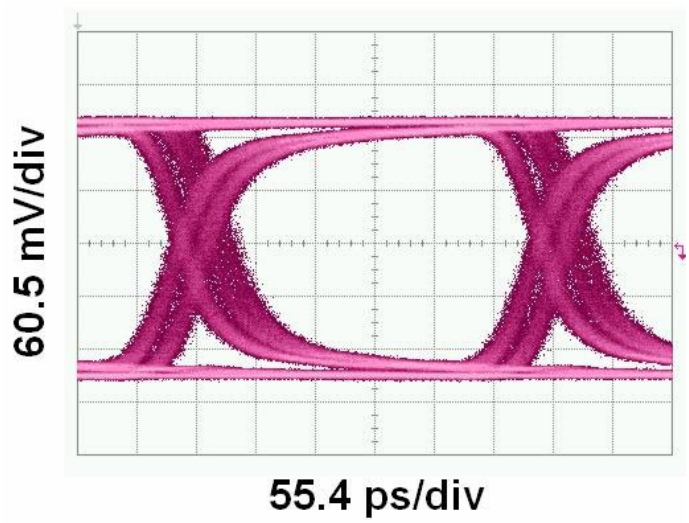

Figure 2.6.6: Measured eye diagram under input optical power of +0dBm at 3Gb/s.

Continued on Page 586

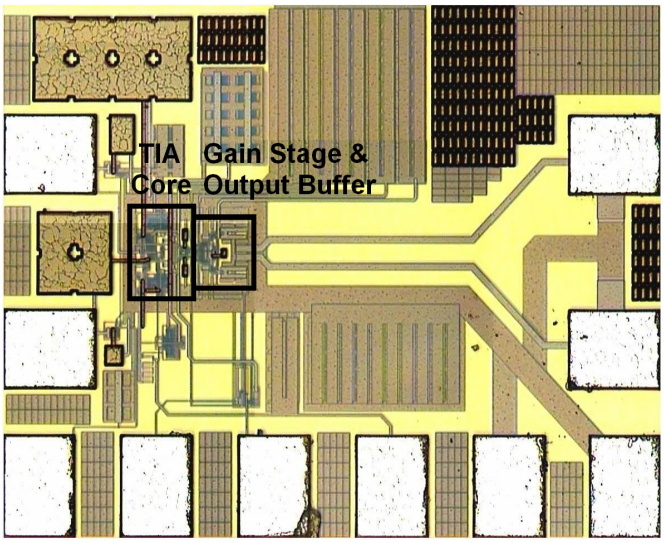

Figure 2.6.7: Die micrograph.

